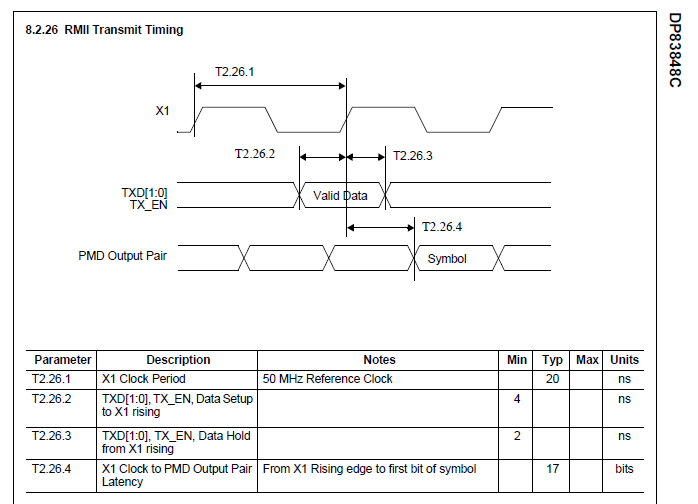
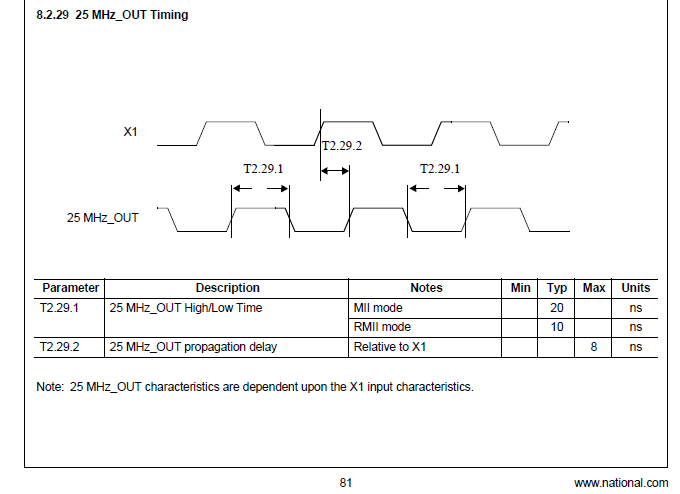
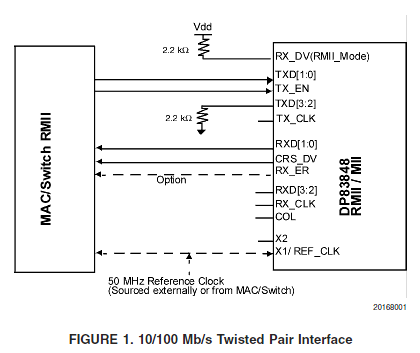
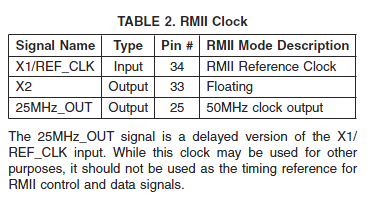
1. Reference Clock (50 MHz):
   1. 
   2. Valid Data time = T2.26.2 + T2.26.3 = 6ns.
   3. 25MHz\_OUT propagation delay = 8ns.

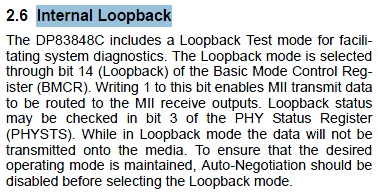


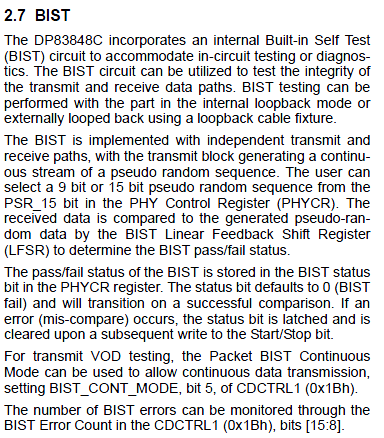
* 1. National Semiconductor. Application Note 1405:





1. Internal Loopback and BIST:





Mail Body

Hi All,

Analysis of the results of the previous stage of debugging revealed:

1. The 25MHz\_OUT signal is a delayed version of the X1/ REF\_CLK input.

While this clock may be used for other purposes, it should not be used as the timing reference for RMII control and data signals (details see in attached file).

2. For proper synchronization MCU and PHY need to:

2.1. Remove resistor R424.

2.2. Connect U1/35 (ETH\_RMII\_REF\_CLK) to U10/34 (oscillator 50MHz).

3. To analyze the efficiency and quality (stability) of it is expedient to use the functions Loopback and BIST of PHY (DP83848C).

4. BIST testing can be performed with the part in the internal loopback mode or externally looped back using a loopback cable fixture.

5. BIST mode and loopback cable fixture will now test the improvements made ​​in the previous step (details see in attached file).

6. We need to verify the absence (if necessary remove) resistors: R423, R426,R427.